**Name: Maaz Habib**

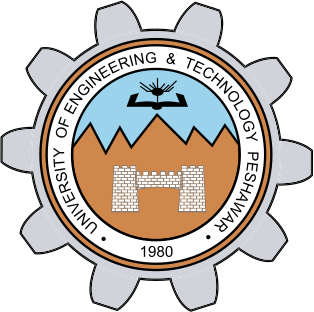
**Roll Number: 20PWCSE1952**

**Section: C**

**Semester: 3rd**

Lab Report Digital Logic Design Lab

Department of Computer Systems Engineering



Submitted to: Mr. Faiz Ullah

# Objective of the Lab:

**Lab # 8**

**“Magnitude Comparators”**

* Realization of 1-bit comparator using logic gates.
* Realization and implementation of 2-bit comparator using logic gates on breadboard.
* Implementation of 4-bit magnitude comparator on breadboard using IC 7485
* Implementation of 8-bit magnitude comparator using two 7485 ICs.

# Components Required:

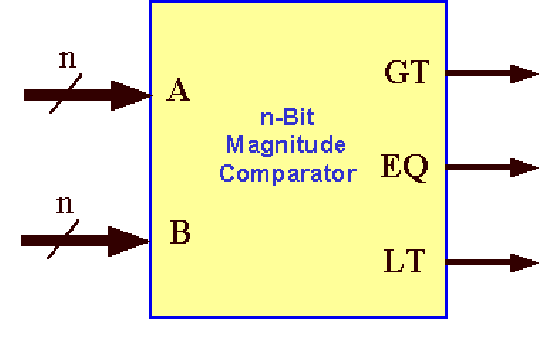
* Breadboard.
* IC type 7486 Quadruple 2-input XOR gates.
* IC type 7408 Quadruple 2-input AND gates.
* IC type 7400 Quadruple 2-input NAND gates.
* IC type 7410 triple 3-input NAND gates.
* IC type 74L85 4-bit magnitude comparator.
* Switches for inputs.
* LED displays for outputs.

# Theory:

**Magnitude Comparator:**

Magnitude Comparator are digital circuits which have two ports which accept and have three single bit outputs. It is used to comparing individual bits, multi-bit comparators can be constructed to compare whole BCD words to produce an output if one word is larger, equal to or less than the other.

### Block Diagram:

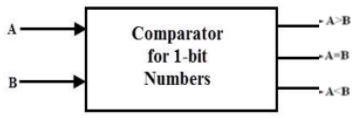
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#### Figure 1: Block diagram of n-bit Magnitude Comparator

**3-bit comparator:**

It is a comparator used to compare two 1-bit binary numbers. It has two binary inputs A, B and three binary outputs: greater than, equal and less than relations.

### Block Diagram:



### Truth Table:

**Expressions:**

#### Figure 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **INPUTS** | | **OUTPUTS** | | |
| **A** | **B** | **A=B** | **A<B** | **A>B** |
| **0** | **0** | **1`** | **0** | **0** |
| **0** | **1** | **0** | **1** | **0** |
| **1** | **0** | **0** | **0** | **1** |
| **1** | **1** | **1** | **0** | **0** |

**Truth table of 1-bit comparator**

The Boolean functions describing the 1-bit magnitude comparator according to the truth table are:

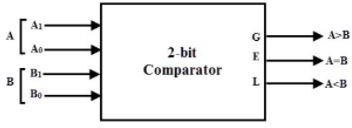
* (𝑨 = 𝑩) = 𝑨̅. 𝑩̅ + 𝑨. 𝑩 = ̅(̅𝑨̅̅̅⊕̅̅̅𝑩̅̅̅)
* (𝑨 < 𝑩) = 𝑨̅. 𝑩
* (𝑨 > 𝑩) = 𝑨. 𝑩̅

# 2-bit Magnitude Comparator:

It is a comparator used to compare two 2-bit numbers. It has 4 binary inputs (number A: A1A0, number B: B1B0) and 3 binary outputs: greater than, equal and less than relations.

### Block diagram:

Figure 4 shows the block diagram of 2-bit magnitude comparator.



### Truth table:

**Expressions:**

#### Figure 4

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **INPUTS** | | | | **OUTPUTS** | | |
| **A1** | **A0** | **B1** | **B0** | **A>B** | **A=B** | **A<B** |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **0** | **0** | **0** | **1** | **0** | **0** | **1** |
| **0** | **0** | **1** | **0** | **0** | **0** | **1** |
| **0** | **0** | **1** | **1** | **0** | **0** | **1** |
| **0** | **1** | **0** | **0** | **1** | **0** | **0** |
| **0** | **1** | **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **0** | **0** | **1** |
| **0** | **1** | **1** | **1** | **0** | **0** | **1** |
| **1** | **0** | **0** | **0** | **1** | **0** | **0** |
| **1** | **0** | **0** | **1** | **1** | **0** | **0** |
| **1** | **0** | **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** | **0** | **0** |
| **1** | **1** | **0** | **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **0** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** | **0** | **1** | **0** |

**Truth table**

Using key-map, the simplified Boolean function for the outputs A>B, A=B and A<B is shown below:

### For A=B:

#### A=B:

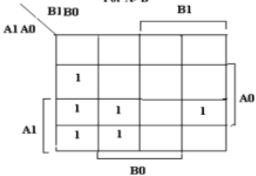
= 𝑨̅𝟏. 𝑨̅𝟎. 𝑩̅𝟏. 𝑩̅𝟎 + 𝑨̅𝟏. 𝑨𝟎. 𝑩̅𝟏. 𝑩𝟎 + 𝑨𝟏. 𝑨̅𝟎. 𝑩𝟏. 𝑩̅𝟎 + 𝑨𝟏. 𝑨𝟎. 𝑩𝟏. 𝑩𝟎

= (𝑨̅𝟏𝑩̅𝟏 + 𝑨𝟏𝑩𝟏). (𝑨̅𝟎𝑩̅𝟎 + 𝑨𝟎𝑩𝟎)

= (𝑨𝟏 ⊕ 𝑩𝟏)′. (𝑨𝟎 ⊕ 𝑩𝟎)′

= 𝑿𝟏. 𝑿𝟎

### For A>B:



#### A>B:

= 𝑨𝟏𝑩′ + 𝑨′ 𝑨𝟎𝑩𝟏′𝑩𝟎′ + 𝑨𝟏𝑨𝟎𝑩𝟏𝑩′

𝟏 𝟏 𝟎

= 𝑨𝟏𝑩′ + 𝑨𝟎𝑩′ (𝑨′ 𝑩𝟏′ + 𝑨𝟏𝑩𝟏)

𝟏 𝟎 𝟏

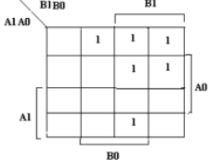
= 𝑨𝟏𝑩′ + 𝑨𝟎𝑩′ (𝑨𝟏⨁𝑩𝟏)′

𝟏 𝟎

= 𝑨𝟏𝑩′ + 𝑿𝟏. 𝑨𝟎𝑩′

𝟏 𝟎

### For A<B:



#### A<B:

= 𝑨𝟏′𝑩𝟏 + 𝑨′ 𝑨𝟎′𝑩𝟏′𝑩𝟎 + 𝑨𝟏𝑨𝟎′𝑩𝟏𝑩𝟎

𝟏

= 𝑨𝟏′𝑩𝟏 + 𝑨𝟎′𝑩𝟎(𝑨′ 𝑩𝟏′ + 𝑨𝟏𝑩𝟏)

𝟏

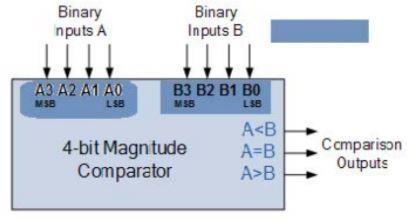
= 𝑨𝟏′𝑩𝟏 + 𝑨𝟎′𝑩𝟎(𝑨𝟏⨁𝑩𝟏)′

= 𝑨𝟏′𝑩𝟏 + 𝑿𝟏. 𝑨𝟎′𝑩𝟏

# 4-bit Magnitude Comparator:

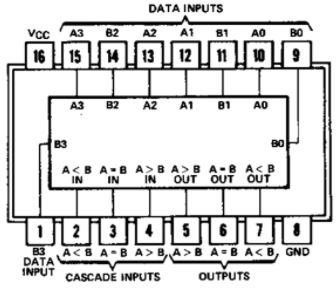
A comparator used to compare two 4-bit words. The two 4-bit numbers are word A: A3A2A1A0, and word B: B3 B2B1B0) so, the circuit has 8 inputs and 3 binary outputs: A>B, A=B and A<B.

**Block Diagram:**



**Pin Description:**

#### Figure 6(a)



**Figure 6(b)**

### Working of 4-bit comparator:

**Equality:**

* Word A equal word B if: A3=B3, A2=B2, A1=B1, A0=B0.

### Inequality:

* If A3 = 1 and B3 = 0, then A is greater than B (A>B). Or
* If A3 and B3 are equal, and if A2 = 1 and B2 = 0, then A > B. Or
* If A3 and B3 are equal & A2 and B2 are equal, and if A1 = 1, and B1 = 0, then A>B. Or
* If A3 and B3 are equal, A2 and B2 are equal and A1 and B1 are equal, and if A0 = 1 and B0 = 0, then A > B.
* If A3 = 0 and B3 = 1, then A is less than B (A<B). Or
* If A3 and B3 are equal, and if A2 = 0 and B2 = 1, then A < B. Or
* If A3 and B3 are equal & A2 and B2 are equal, and if A1 = 0, and B1 = 1, then A<B. Or
* If A3 and B3 are equal, A2 and B2 are equal and A1 and B1 are equal, and if A0 = 0 and B0 = 1, then A < B.

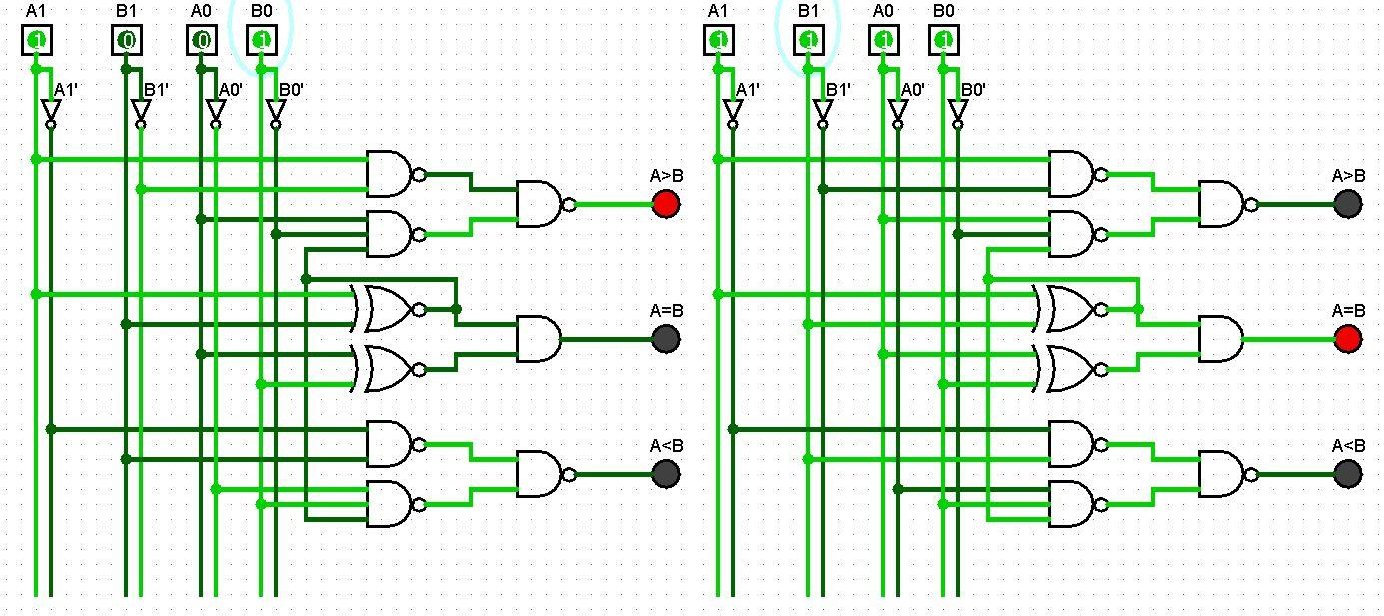
# Lab Tasks:

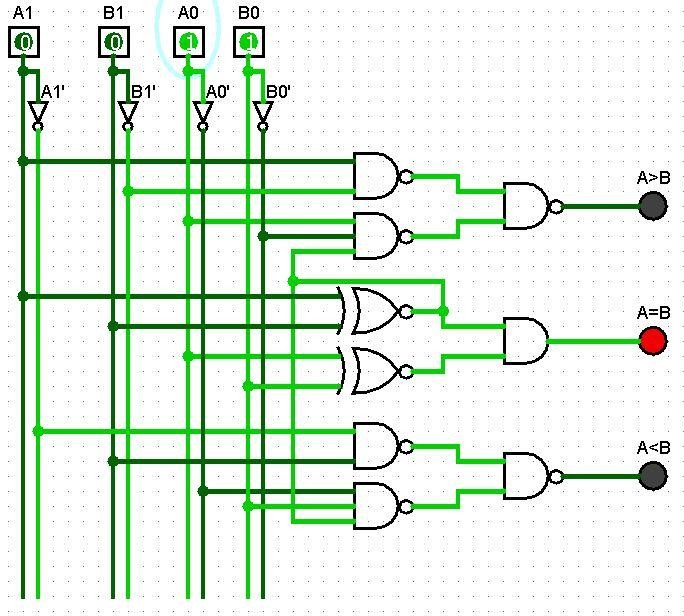
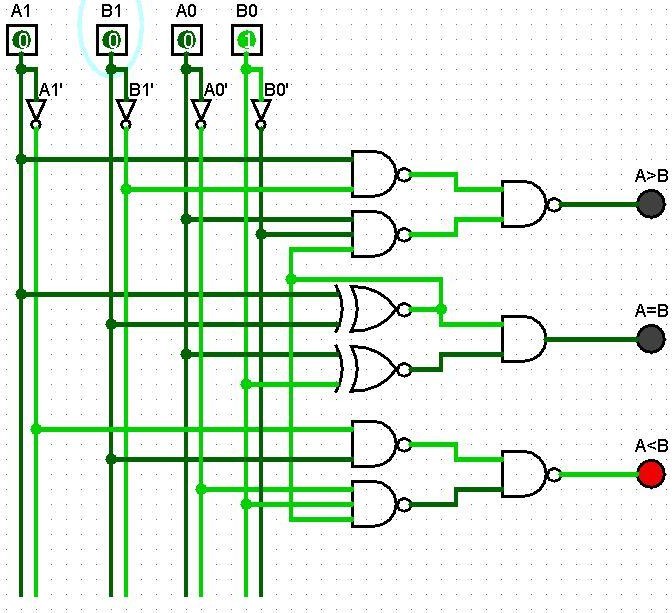
**Part A:**

## Procedure:

* Check all the components for their working.
* Insert the appropriate ICs into the IC base.
* Make connections as shown in the circuit diagram in figure 5.
* Verify the Truth Table and observe the outputs.
* Repeat the same steps but for the circuit diagram in figure 6 and apply inputs in the table. Record the outputs for the given values of A and B.





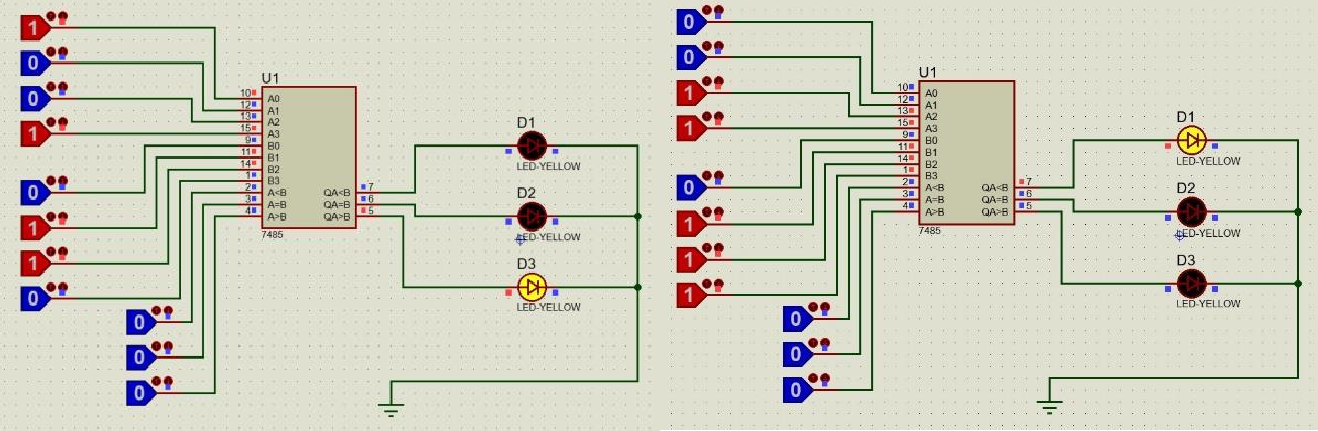


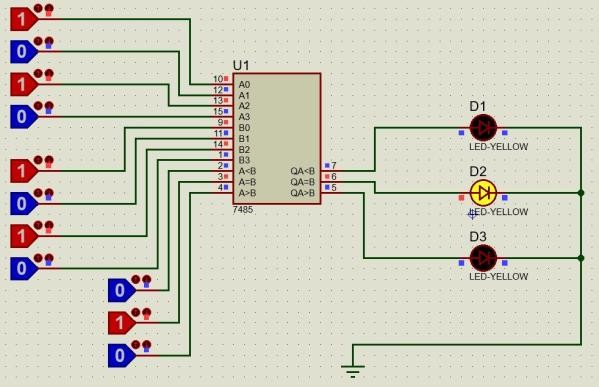
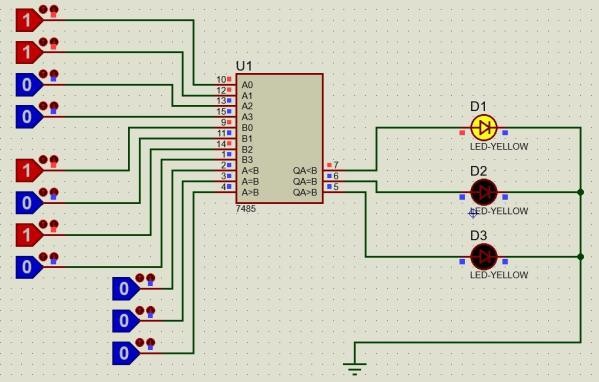
## Table:

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| **A** | **B** |  |
| **10** | **01** | A>B |
| **11** | **11** | A=B |
| **00** | **01** | A<B |
| **01** | **01** | A=B |



**For 4-bit Magnitude Comparator:**





## Table:

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| **A** | **B** |  |
| **1001** | **0110** | A>B |
| **1100** | **1110** | A<B |
| **0011** | **0101** | A<B |
| **0101** | **0101** | A=B |

**Conclusion:**

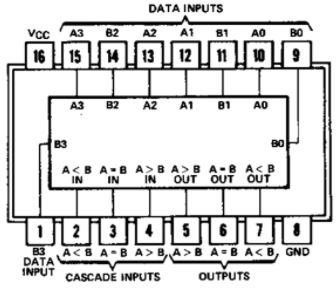
So, Magnitude Comparator is studied.



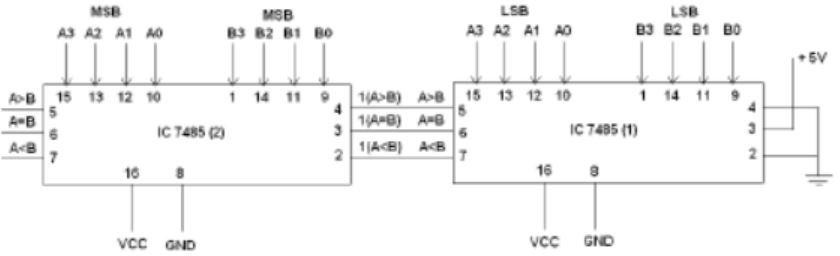
# Part b:

* Design an 8-bit comparator using two chips of IC 7485. The connections are given below.
* Verify the given truth table.

## Pin description:



**Logic diagram for 8-bit Magnitude Comparator:**



## Truth Table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **INPUTS** | | **OUTPUTS** | | |
| **A** | **B** | **A>B** | **A=B** | **A<B** |
| **0000 0000** | **0000 0000** | **0** | **1** | **0** |
| **0001 0001** | **0000 0000** | **1** | **0** | **0** |
| **0000 0000** | **0001 0001** | **0** | **0** | **1** |

**Verification of Truth Table:**

